A 5.8-GHz Two-Stage High-Linearity Low-Voltage Low Noise Amplifier in a 0.35-μm CMOS Technology

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Abstract — **A 5.8-GHz two-stage high-linearity low-voltage CMOS low-nose amplifier (LNA) has been developed in a 0.35-μm pure digital CMOS technology without any additional mask or post-processing steps. A two-stage architecture is used to simultaneously optimize the gain and noise performance. Based on the modified CMOS model valid for RF range, the LNA with fully on-chip input, output and inter-stage matching was designed to verify the two-stage LNA architecture. This LNA chip achieves measured results of 3.2-dB NF, +6.7-dBm IIP3 and -3.7-dBm output P_{1dB} at 5.8 GHz. A figure-of-merit for linearity (output IP3/P_{DC}) of 1.2 is achieved, which is believed to be among the best reported for a CMOS low-noise amplifier operating at 5-6 GHz ISM band. The effective circuit area is only 0.63 x 0.46 mm^2.**

I. INTRODUCTION

The demand on high bit-rate wireless LAN systems is driven by the growing popularity of notebook computers. To provide data rates of several tens of megabits per second in wireless LAN systems, OFDM based WLAN modulation in the 5-6 GHz ISM band becomes very popular. OFDM based WLAN modulation is very challenging to RF front-end circuits about the linearity and dynamic range. Besides, to operate in wideband wireless portable systems, low-voltage low-power RF circuits are required. The design of such circuits is therefore a key issue and LNA is the most important component in the receiver chain.

LNAs using high performance processes were designed [1]-[7]. However, due to the advantages of low cost and integration ability with baseband circuits, the CMOS RF chips are getting more and more attractive. LNAs using 0.24-μm CMOS processes have demonstrated good gain and noise performance in the 5-6 GHz ISM band [8]. To achieve such performance, however, a costly RF-enhanced CMOS process is required and the power consumption and the power supply requirement are very large. A 2V LNA using 0.24-μm CMOS process with 7.2-mW power consumption [9] and an LNA using 0.35-μm CMOS process [10] were designed but the noise performance is degraded seriously. An alternative low-voltage topology using a planar-interleaved transformer was depicted using 0.35-μm CMOS process [11]. However, the low-Q transformer contributes significant resistance in the RF range, which not only reduces the gain but also increases the noise figure (NF). Besides, the linearity is degraded due to the use of the cascode architecture in the previous circuits. In this paper, to simultaneously achieve high performance, high linearity, low supply voltage, low power consumption, a 5.8-GHz two-stage low-nose

Process	Freq. (GHz)	Circuit Area without pads (mm^2)	NF (dB)	Gain (dB)	IIP3 (dBm)	Input P_{1dB} (dBm)	Output IP3/P_{DC}	Power Supply	P_{DC} (mW)	Design Features	Ref.
0.7μm MESFET	5.2	0.4 x 1.1	3.5	15	NA	-21	NA	3.3	10	Two-stage CS	[1]
GaAs HBT	5.7	0.5 x 0.6	2.9	16	7.3	-5.7	3.0	3.5V	72	Two-stage R-feedback	[2]
SiGe HBT	5.8	0.5 x 0.6	2.1	6.9	-11	-21	0.03	1V	13	Two-stage CE	[3]
Si Bipolar	5.8	0.45 x 0.45	4.2	7	-4	NA	0.3	3.5V	7.7	CC L-degeneration	[4]
0.6μm Si Bipolar	5.8	0.45 x 0.45	4.1	16	NA	-15	NA	5V	100	Two-stage CE	[5]
0.8μm BiCMOS	5.8	0.91 x 0.56	3.3	6.9	NA	NA	NA	3V	9	Single-stage CE	[6]
0.5μm Si Bipolar	5.8	0.84 x 0.57	4	11.5	NA	-19	NA	1V	6.6	LC-tank CC	[7]
0.24μm CMOS	5.25	0.83 x 0.39	2.5	16	-1.5	-11.7	0.6	3V	48	Differential CC	[8]
0.24μm CMOS	5.2	0.8 x 0.5	4.8	18 (v/v)	-2	-14	NA	2V	7.2	Differential negative R	[9]
0.35μm CMOS	5.8	1.12 x 0.94	4	5	NA	NA	NA	3.3V	50	Differential CS	[10]
0.35μm CMOS	5.2	1.06 x 0.54	5.6	7.8	2.8	-6.2	0.9	1V	12.2	Interleaved transformer	[11]
0.35μm CMOS	**5.8**	**0.63 x 0.46**	**3.2**	**7.2**	**6.7**	**-3.7**	1.2	**1.3V**	**20**	**two-stage CS**	**This work**

Table. 1. Recently reported performance of 5-6GHz ISM band low noise amplifiers. Effective circuit areas without pads are estimated *from the die photograph.* (CC: Cascode topology. CS: Common-source topology. CE: Common-emitter topology).

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amplifier architecture was designed in a 0.35-μm pure digital CMOS technology without any additional mask or post-processing steps. Table 1 summarizes the recently reported performance of 5-6 GHz ISM band low noise amplifiers compared with this work. Our chip demonstrated the best output IP3/P_{DC} with a miniature effective chip size among the previous reported CMOS LNAs at this frequency.

II. 5.8-GHz Two-Stage LNA Circuit Design

The performance of the sensitivity of a communication system is heavily determined by a LNA. A system noise figure is defined as

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \quad (1)$$

where F_1, F_2, F_3, ... is the noise factor of each stage, G_1, G_2, G_3, ... is the gain of each stage

The typical CMOS LNA circuit topology is cascode with the inductor degeneration. Since the drain of the common-source stage is terminated with the source of the common-gate stage, the gain of the common-source stage is relatively small and the total noise performance will be degraded by the noise of the common-gate stage according to (1). Besides, the unit-gain frequency of the device depends on not only the overdriving voltage (V_{gs} - V_t) but also drain-source voltage (V_{ds}). To provide enough unit-gain frequency to achieve noise and gain performance, higher value of V_{gs} and V_{ds} are needed, which not only increases the supply voltage (Vdd) but also degrades the linearity.

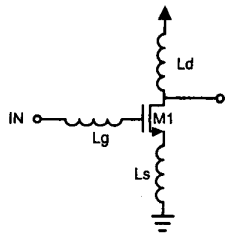

Fig. 1. Common-source LNA topology.

To achieve high linearity, low supply voltage, and avoid noise performance degradation, a common-source topology is adopted as in Fig. 1. The input matching condition and noise performance of an inductor-degeneration topology with ideal inductors was fully analyzed in [12]. Due to the low Q of the inductors in the 0.35-μm CMOS technology, the parasitic resistance has to be considered. The input impedance is

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + R_g + R_{Lg} + R_{Ls} + \frac{g_{m1}}{C_{gs1}} L_s \quad (2)$$

where C_{gs} is the gate-source capacitance and g_{m1} is the transconductance of device M1. R_g is the effective gate resistance. R_{Lg} and R_{Ls} are the parasitic resistance of the inductors L_g and L_s and are approximately proportional to L_g and L_s, respectively. The matching condition occurs when

$$\omega^2 C_{gs}(L_g + L_s) \approx 1 \quad (3)$$

$$R_s \approx R_g + R_{Lg} + R_{Ls} + \frac{g_{m1}}{C_{gs}} L_s \quad (4)$$

where ω is the center frequency in radians/s. With these conditions, the LNA noise factor F can be show to be

$$F \approx 1 + \frac{R_g}{R_s} + \frac{R_{Lg}}{R_s} + \frac{R_{Ls}}{R_s} + \gamma g_{d0} R_s (\frac{\omega}{\omega_t})^2 \quad (5)$$

where g_{d0} is the zero-bias drain conductance of the device, and γ is a bias-dependent factor [13].

The noise figure of LNA becomes high value when the value of L_g is increases. Besides, because the spiral inductor is not ideal, the parasitic resistance of the inductor will degrade the noise figure. Hence, based on (1)-(3), it is hard to simultaneously optimize gain and noise performance with constrained power consumption.

A two-stage topology is used to simultaneously optimized the gain and noise performance as in Fig. 2. The first stage is designed for noise performance and the second stage is designed for gain. The maximum power gain is obtained when $\Gamma_s = \Gamma_{IN}^*$ and $\Gamma_L = \Gamma_{out}^*$ with the inductors L_m, L_{gnd} and L_o. The two stage are complex conjugate matched by the interstage inductor L_m.

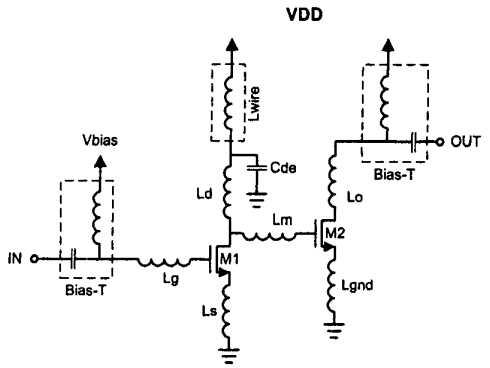

Fig. 2. Proposed topology of two-stage low-voltage CMOS LNA.

On-chip decoupling capacitor C_{de} is used as a RF-short in the VDD to filter out the high frequency power supply noise and to rid of the influence of the parasitic inductance

of the bonding wire or the DC probe. 200μm/0.35μm and 100μm/0.35μm MOSFETs are used in the first and second stages respectively for the power consumption consideration. Due the high sheet resistance of poly gate of the MOSFET, a multi-finger structure with 5μm finger length was used in each MOSFET to reduce the gate resistance such that R_g in (5) can be reduced and the noise performance could be improved.

III. RF Models and Layout Consideration

The modified MOSFET model for simulation is based on the BSIM3v3 SPICE model, with some passive components added to take account of the parasitic effects in the RF range. Besides, although RF-enhanced CMOS processes provide a thick top metal to enhance the Q-factor of the spiral inductor and a thin oxide layer to increase the value of the capacitor, these needs a additional masks and are not standard processes for pure digital CMOS.

The inductors were modeled as a lump-circuit network and the parameters were extracted by experimental measurements. The Q-factor of on-chip spiral inductor is quite low due to its parasitic effects. In order to reduce the loss in the metal conductance of a spiral inductor, a hollow spiral inductor is used to increase the value of Q [14] and the top three metal layers are shunted to reduce parasitic resistance of the inductor as in Fig. 3.

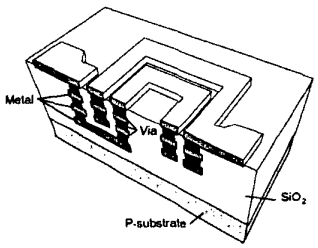

Fig. 3. The top three metal layers are shunted to reduce the parasitic resistance of the inductor.

The large decoupling capacitor was designed with a interleaved metal capacitor instead of a MOS capacitor due to noise and linearity consideration as in Fig. 4, and the spare area was made full use of to reduced area. To prevent unexpected stability problems and noise, all blank area was covered with fully connected "ground" but the neighborhood of the passive and active devices to reduce extra parasitic effects.

The layouts of all devices remain the same as the test keys to coincide with the measurement. For accuracy, the parasitic effect of each interconnection was carefully calculated and included in the post-layout simulation.

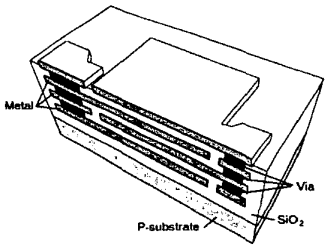

Fig. 4. The decoupling capacitor was constructed with interleaved metals.

IV. Measurement Results

The proposed two-stage low-voltage CMOS LNA was fabricated using a 0.35-μm 1P4M standard digital CMOS process, which provides single poly layer for the gates of the MOS and four metal layers for interconnection. A die micrograph is shown in Fig. 5. The chip size is 0.88x0.74 mm^2 and the effective circuit area without pads is only 0.63x046 mm^2. The circuit was tested via on-wafer probing. Fig. 6 shows the measured S-parameters and noise figure. The measured values were as follows: |S11| is −11dB, |S22| is −17dB, |S21| is 7.2dB and NF is 3.2dB at 5.8 GHz, with 15mA drawn form the 1.3V supply voltage without any off-chip tuning. The measurement result of a two-tone third order intercept point (IP3) with 5.8-GHz and 5.85-GHz inputs was showed as in Fig. 7. The input-referred IP3 is +6.7dBm and the measured input-referred P_{1dB} is -3.7dBm. The relatively low gain performance of the LNA is due to the on-chip low-Q spiral inductors and the tradeoffs of bias for low noise and dc power consumption.

V. Conclusion

A two-stage high-linearity low-voltage low-noise amplifier topology using low-cost 0.35-μm CMOS process has been demonstrated. This 1.3V 5.8-GHz CMOS LNA has been designed, fabricated and tested. The measurement results prove that the proposed CMOS LNA topology can achieve the demand of low noise and high linearity with low supply voltage at a high frequency. Since this LNA was fabricated using standard 0.35-μm CMOS technology, it can be easily integrated with other front-end circuits to built CMOS transceivers without requiring any additional mask or post-processing steps.

ACKNOWLEDGEMENT

This work is supported in part by National Science Council, ROC (contact no. NSC 89-2213-E-002-178, NSC 89-2219-E-002-042) and the Research Excellence Program funded by Ministry of Education, ROC (ME 89-E-FA06-2-4). The chip is fabricated by TSMC through the Chip Implementation Center (CIC), Taiwan, ROC. The authors would like to thank K. L. Deng, P. Y. Chen and National Nano-Device Laboratory (NDL), Taiwan, ROC, for the chip testing. Thanks also go to Prof. Y. J. Chan of National Central University for providing CMOS RF models.

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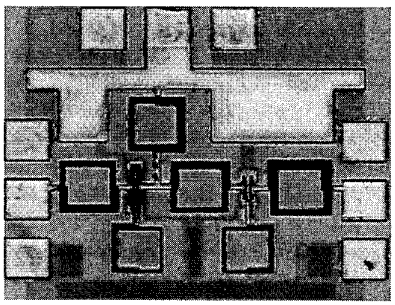

Fig. 5. Die photograph of proposed two-stage CMOS LNA.

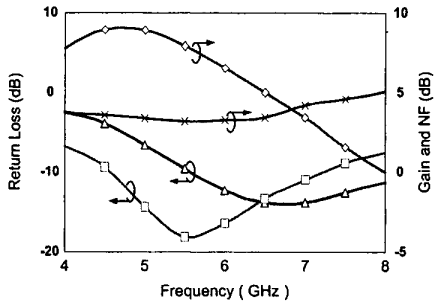

Fig. 6. Measurement results of proposed two-stage CMOS LNA.
◇ S21 (|S21| = 7.2dB at 5.8GHz)
△ S11 (|S11| = -11dB at 5.8GHz)
○ S22 (|S22| = -17dB at 5.8GHz)
x Noise Figure (NF = 3.2dB at 5.8GHz)

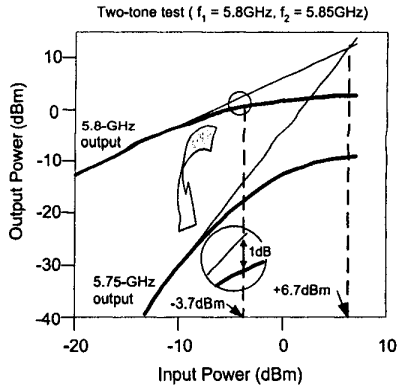

Fig. 7. 1-dB compression point and third order intercepts point measurement